WHAT IS CLAIMED IS:

1. A split gate-type SONOS device comprising:

a substrate;

a first impurity region and a second impurity region formed in the substrate, separated by a first channel region and a second channel region;

a control gate crossing over the first channel region and the second channel region; and

a tunnel insulating layer, a charge storing layer, and a gate interlayer insulating layer interposed between the control gate and the substrate in the first channel region, wherein the gate interlayer insulating layer is interposed between the control gate and the substrate in the second channel region, and wherein the first channel region and the first impurity region are wider than the second channel region and the second impurity region, respectively.

2. A split gate-type SONOS device as claimed in claim 1, wherein the first impurity region is a drain region and the second impurity region is a source region.

3. A split gate-type SONOS device as claimed in claim 1, wherein the sides of the tunnel insulating layer, the charge storing layer, and the gate interlayer insulating layer are aligned with the side of the control gate.

4. A split gate-type SONOS device as claimed in claim 1, wherein the control gate is formed of polycrystalline silicon.

5. A split gate-type SONOS device as claimed in claim 1, wherein the charge storing layer is formed of silicon nitride.

6. A split gate-type SONOS device as claimed in claim 1, wherein the tunnel insulating layer is formed of silicon oxide.

7. A split gate-type SONOS device as claimed in claim 1, wherein the gate interlayer insulating layer is formed of silicon oxide.

8. A method of fabricating a split gate-type SONOS device, the method comprising:

forming a field region in a substrate, where the field region defines a wide active region and a narrow active region, wherein the narrow active region has a width narrower than the wide active region;

forming a tunnel insulating layer and a charge storing layer pattern stacked on a section of the wide active region;

forming a control gate crossing over the charge storing layer pattern in the wide active region, and over a section of the narrow active region; and

injecting impurities into the active regions on both sides of the control gate to form a first impurity region and a second impurity region.

9. A method as claimed in claim 8, further comprising forming a gate interlayer insulating layer disposed between the control gate and the charge storing layer pattern in the wide active region, and disposed between the control gate and the substrate in the narrow active region.

10. A method as claimed in claim 8, wherein the control gate is formed of polycrystalline silicon.

11. A method as claimed in claim 8, wherein the charge storing layer is formed of silicon nitride.

12. A method as claimed in claim 8, wherein the tunnel insulating layer is formed of silicon oxide.

13. A method as claimed in claim 9, wherein the gate interlayer insulating layer is formed of silicon oxide.

14. A nonvolatile memory device, comprising:

first and second impurity regions on a substrate separated by a first channel region and a second channel region, said first channel region being wider than said second channel region and said first impurity region being wider than said second impurity region.

15. The device recited in claim 14, further comprising a tunnel insulating layer, a charge storing layer, and a gate interlayer insulating layer disposed on the substrate in said first channel region.

16. The device recited in claim 15, wherein said gate interlayer insulating layer extends over the substrate in the second channel region.

17. The device recited in claim 15, further comprising a control gate disposed over said first and second regions.

18. The device recited in claim 17, wherein said control gate is formed of polycrystalline silicon, said charge storing layer is formed of silicon nitride and said tunnel insulating layer is formed of silicon oxide.

19. The device recited in claim 14, further comprising:

a control gate crossing over said first channel region and said second channel region; and

a tunnel insulating layer, a charge storing layer, and a gate interlayer insulating layer interposed between said control gate and said substrate in the first channel region, wherein the gate interlayer insulating layer is interposed between the control gate and the substrate in the second channel region.

20. A method of fabricating a nonvolatile memory device, the method comprising:

forming a wide active region and a narrow active region on a substrate,

forming a charge storing layer pattern on a section of the wide active region;

forming a control gate crossing over the charge storing layer pattern in the wide active region, and over a section of the narrow active region; and

injecting impurities into the active regions on both sides of the control gate to form a first impurity region and a second impurity region.

21. The method recited in claim 20, further comprising forming a field region to define said wide and said narrow active regions.

22. The method recited in claim 20, further comprising forming a tunnel insulating layer on a section of the wide active region.

23. The method recited in claim 20, further comprising forming a gate interlayer insulating layer between said control gate and said charge storing layer pattern.